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5 METHOD AND APPARATUS FOR JITTER MEASUREMENT USING PHASE
AND AMPLITUDE UNDERSAMPLING

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No.
10 60/461,933, filed April 10, 2003 and U.S. Provisional Application No. 60/477,520, filed
June 11, 2003. The entire teachings of the above applications are incorporated herein
by reference.

BACKGROUND

15 Jitter has been defined as the short-term non-cumulative variations of the
significant instants of a clock or data signal from their ideal positions in time. The
significant instants can be the rising or falling edge of a pulse. Jitter has a variety of
sources including imperfections in oscillators, thermal noise, instabilities in the
oscillator electronics, RF interference and the transmission of signals through
20 communications equipment such as regenerative repeaters. Large amounts of jitter can
cause equipment to fail; hence, designers must look to jitter measurement techniques
and devices to properly address the effects of jitter.

Two basic methods may be employed to measure jitter and its effects on
equipment: the oscilloscope method and the phase detector method. According to the
25 oscilloscope method a first clock source provides a jitter-free trigger signal for an
oscilloscope and the first clock's frequency reference is locked to a second clock
source. The second clock source is modulated by jitter and input to a pattern generator

which provides jittered data to equipment being tested. The input and output
waveforms to the equipment may then be analyzed with oscilloscope functions. Also,
the oscilloscope may be used to view eye patterns of signals. The oscilloscope method,
however, is limited to jitter having amplitudes less than one unit interval (one unit

5   period).

According to the phase detector method, the phase of the recovered clock,
output from the equipment receiving a data signal having jitter, is compared with the
phase of the jitter-free clock source. The resulting phase difference is the jitter
amplitude measured in unit intervals. A frequency divider placed between the

10   recovered clock signal and the phase detector extends the range of phase detector
beyond the unit interval.

Accurately measuring jitter has become increasingly important in testing
communications components that operate at high bit rates. As bit rates increase with
developing fiber optic technology, jitter increases causing communication components

15   to malfunction. Thus, accurate jitter measurements are necessary for designers to
account for jitter. However, measuring the jitter of a high bit rate signal requires the use
of costly sampling hardware (e.g., gallium arsenide semiconductor technology).

SUMMARY

20   Phase and amplitude under-sampling may be employed to measure jitter and
avoid the use of costly sampling hardware required for high bit rate signals. In an
embodiment, according to the present approach, a jitter measurement device includes a
sampling circuit, a computation circuit, and a signal processor. The sampling circuit
samples an input signal and provides amplitude and phase information to the

25   computation circuit which uses the information to compute Time Interval Error (TIE)
information. The signal processor processes the TIE information to produce a jitter
spectrum.

In one aspect, a signal characteristics circuit extracts characteristics from the
input signal prior to jitter measurements for use by the computation circuit in computing

30   TIE information. An embodiment of the signal characteristics circuit includes: a

wideband clock recovery block that extracts a synchronous clock from the input signal, a narrowband programmable Phase Lock Loop (PLL) that generates a sample clock from the synchronous clock, a sampler that samples the input signal using the sample clock, an Analog to Digital (A/D) converter that converts the input signal samples to

5 digital data, and a Digital Signal Processor (DSP) that determines signal characteristics from the digital data.

The narrowband programmable PLL includes a reference divider that receives a recovered clock signal from the wideband clock recovery block, a Voltage Controlled Oscillator (VCO), a feedback divider that receives the output from the VCO, a phase

10 detector that receives the outputs from the reference and feedback dividers, and a filter that connects the output from the phase detector to the input of the VCO.

The DSP of the signal characteristics circuit is operable to determine high and low values from the digital data to provide high and low threshold values. The DSP further groups the digital data based on whether the digital data is associated with rising

15 or falling edges of the input signal, averages the digital data in both groups that falls within the high and low threshold values, and stores the result in appropriate look up tables corresponding to the rising or falling edge groups.

In an embodiment, the sampling circuit includes a Track and Hold (T/H) sampler that samples the input signal according to the sample clock delayed by a fixed

20 delay. An A/D converter converts the amplitude samples into quantized amplitude values. In addition, one flip-flop receives the sample clock delayed by an adjustable delay and a fixed one unit delay and another flip-flop receives the sample clock delayed by an adjustable delay. In this way the pair of flip-flops sample the input signal to obtain digital sample values positioned in time both before and after the amplitude

25 sample. The adjustable delay may further be adjusted such that the digital samples occur one half of a unit interval before and after the amplitude sample. Relocating the adjustable delay to a position between the sample clock and the T/H sampler can achieve the same result. These digital sample values describe the phase corresponding to the amplitude sample. The flip-flops may also be thermally coupled with a heat sink

30 to maintain their timing requirements over a wide temperature range.

Another embodiment obtains the phase and amplitude information using two
T/H samplers, a comparator, and an A/D converter. The T/H samplers sample the input
signal according to sample clocks separated by a one half unit interval delay and
provide the resulting amplitude samples to a comparator which outputs phase

5   information. A quantized amplitude value is obtained by applying the output from one
of the T/H samplers to an A/D converter. In another embodiment the outputs from the
T/H samplers may both be applied to separate A/D converters to produce two quantized
amplitude values. The DSP can compute phase information from the two quantized
amplitude values without the need of a comparator.

10   The computation circuit uses the quantized amplitude value as an address to
obtain a current measured index from the lookup table corresponding to the phase
information. The computation circuit further computes a current ideal index by adding
a previous ideal index to the fractional part of the decimal number obtained by
multiplying a ratio of the input signal frequency to the sampling clock frequency by the

15   sample order of the input signal data registered in an internal counter. Unique samples
of the input signal may be acquired by ensuring that the inverse of the ratio of the input
signal frequency to the sampling clock frequency is a prime fraction. The computation
circuit finds the difference between the current measured index and the current ideal
index. The result is TIE information which may be analyzed by the signal processor to

20   determine peak-to-peak jitter or a ratio of random to deterministic jitter.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will
be apparent from the following more particular description of preferred embodiments of

25   the invention, as illustrated in the accompanying drawings in which like reference
characters refer to the same parts throughout the different views. The drawings are not
necessarily to scale, emphasis instead being placed upon illustrating the principles of
the invention.

Fig. 1 shows a block diagram of a general embodiment of the present invention.

Fig. 2 shows a circuit block diagram of an embodiment of the extract signal characteristics block in Fig. 1 that includes a narrowband phase lock loop (NPLL).

Fig. 3 shows a block diagram for the NPLL of Fig. 2.

Fig. 4 illustrates a diagram showing the ideal rising and falling edge signal characteristics.

Fig. 5 shows a circuit block diagram of another embodiment of the extract signal characteristics block in Fig. 1 that includes a programmable Direct Digital Synthesizer.

Fig. 6 shows a block diagram of the DDS of Fig. 5.

Fig. 7 illustrates a timing diagram and DSP algorithm for the coherent under-sampling circuit used in Fig. 1 to extract signal characteristics.

Fig. 8A shows a block diagram of an embodiment of the sampling circuit shown in Fig. 1.

Fig. 8B illustrates possible positions of the sampling instants with respect to the input signal.

Fig. 9 shows a block diagram of an athermal embodiment of the sampling circuit shown in Fig. 1.

Fig. 10 shows a timing diagram of the sampling circuit shown in Fig. 9.

Fig. 11 shows another timing diagram of the sampling circuit shown in Fig. 9.

Fig. 12 shows a state table and an illustration of each of the states for the state machine implemented in the statistics counter shown in Fig. 1.

Fig. 13 shows a block diagram of a second athermal embodiment of the sampling circuit shown in Fig. 1.

Fig. 14 shows a block diagram of a third athermal embodiment of the sampling circuit shown in Fig.1.

Fig. 15 shows a block diagram of the Time Interval Computation and Signal Processing blocks shown in Fig. 1.

Fig. 16 shows an algorithm corresponding to the Time Interval Computation block diagram shown in Fig. 15.

DETAILED DESCRIPTION OF THE INVENTION

A description of preferred embodiments of the invention follows.

5   Fig. 1 shows a block diagram of a jitter measurement circuit in accordance with the principles of the present invention. The jitter measurement circuit includes a block to extract signal characteristics 105, a sampling circuit 140, a delay control circuit 120 consisting of a statistics counter 125 and a Proportional-Integral-Derivative (PID) controller 130, a time interval computation block 160, and a signal processing block

10   180.

Before taking jitter measurements, the extract signal characteristics block 105 samples an input signal using the coherent undersampling technique and averages the result to obtain "ideal" rising and falling edge waveforms. To begin jitter measurements an amplitude asynchronous under-sampler 145 and a phase/transition

15   sampled identifier 150 receive the input signal and output amplitude and phase information corresponding to the input signal. The statitistics counter 125 processes the amplitude and phase information to determine how much the delay on the sample clock driving the amplitude asynchronous under-sampler should be adjusted such that the amplitude is sampled within thresholds of a rising or falling edge of the input signal.

20   The statistics counter provides processed phase and amplitude information to the PID controller 130 which adjusts the delay appropriately.

A time interval extraction block 165 receives the amplitude and phase information and computes a time interval. The time interval error extraction block 170 receives the time interval information and computes a time interval error (TIE) which is

25   accumulated, using an accumulator 175, to produce TIE sequence information. TIE is defined as the phase difference between the signal being measured and the sample or reference clock. A digital signal processor (DSP) 185 processes the TIE sequence information and provides various characteristics of the measured jitter including a maximum TIE (TIE_Max), a jitter spectrum, or a ratio of random to deterministic jitter

(Rj/Dj). Maximum TIE is defined as the largest peak-to-peak TIE in any observation interval

An embodiment of the signal characteristics extraction block 105 is shown in more detail in Fig. 2. The signal characteristics extraction block 105 includes a

5 wideband clock recovery block 210, a programmable Narrowband Phase Lock Loop (NPLL) 220, a sampler 230, an Analog to Digital (A/D) converter 240, and a Digital Signal Processor (DSP) 250. These blocks form an embodiment of a coherent under-sampling circuit.

According to coherent undersampling as it applies to the present invention, a

10 clock signal is derived from the input signal, frequency divided, and applied to the sampler 230 which samples the input signal at a rate less than the Nyquist rate (two times the highest frequency of the signal). Usually, undersampling causes aliasing such that the samples incorrectly represent the sampled signal. In the present invention, however, since the sample clock is synchronized with the input signal so that unique

15 samples of the input signal are obtained, the input signal characteristics may be correctly reconstructed. Coherent undersampling has the advantage of requiring less expensive sampling hardware operating at lower sampling frequencies.

The wideband clock recovery block 210 extracts a synchronous clock from the incoming input signal. The wideband clock recovery can be implemented using an off

20 the shelf device such as a Broadcom BCM8129 or other similar commercial device.

The programmable NPLL 220 is shown in more detail in Fig. 3 and includes a reference divider 310, a charge pump phase detector 320, a filter 330, a hi-Q Voltage Controlled SAW (Surface Acoustic Wave) Oscillator (VCSO) 340, and a feedback divider 350. The filter 330 can be a low pass filter or a band pass filter. The

25 programmable NPLL cleans up phase noise and jitter that are characteristics of the recovered clock and generates a sample clock. The sample clock has a frequency relationship to the recovered clock given by the following equation:

Sample Clock= Recovered Clock * M / N

30

where M and N are input values for the feedback and reference dividers associated with the sampling clock and the recovered clock, respectively. The ratio of M/N is preferably a prime fractional number. The prime fractional ratio ensures unique samples over one cycle of the incoming signal.

5   The embodiment of Fig. 2 may have certain limitations with respect to the resolution of the frequency, due to the limits of the M and N values to a practical number. Large M and N values result in a very low intermediate frequency of the phase detector, which may cause instability in the locking process of the PLL, and can also be limited in terms of the supported bit rates.

10   Referring again to Fig. 2, the sampler 230 takes a snap shot of the input signal upon receiving a clock signal, namely the "Sample Clock." The sampler can be realized using an off the shelf device such as the Rockwell Scientific RTH-020.

The A/D converter 240 converts the sampled analog value of the incoming signal to a digital value that is interpreted by the DSP. The A/D converter 240 can be

15   realized with numerous off the shelf commercial devices, such as an Analog Devices AD9430.

The DSP 250 implements an algorithm that constructs ideal rising and falling edge signal characteristics, LH_Ideal 410 and HL_Ideal 420, shown in Fig. 4, from the various snapshots taken of the incoming signal. The algorithm assigns (x,y) coordinates

20   for each sample, wherein x 440 represents the time domain axis within a unit interval and y 430 represents the signal amplitude. Samples that are within preset high and low thresholds are accumulated over time and grouped according to rising and falling edges. The algorithm averages each group's data over the unit interval and stores the result in memory or look up tables as shown in Fig. 15. The algorithm further determines from

25   the samples average high and low values, High and Low, and stores the values in local memory for comparison with captured data in Time Interval Error (TIE) measurements described further herein. Lastly, the algorithm produces a signal, Tune_DC, to tune the delay control circuit 120 shown in Fig. 1.

Fig. 5 shows a circuit block diagram of another embodiment of the extract signal

30   characteristics block 105 that includes a programmable Direct Digital Synthesizer

(DDS) 520 for providing coherent under-sampling. In addition to the wideband clock recovery block 210, sampler 230, A/D converter 240, and DSP 250 already described, the embodiment of Fig. 5 includes a Fixed Multiplier & Cleanup PLL 525 and a DDS Fractional Divider 520.

5   The Fixed Multiplier & Cleanup PLL 525 is a particular implementation of the programmable NPLL 220 described above, with specific features that include narrower loop bandwidth, fixed values for reference and feedback dividers, and higher Q. These PLL characteristics result in lower phase noise and lower intrinsic jitter generation, critical for reducing jitter uncertainties for eye measurements. This embodiment

10 requires that a fixed input frequency be used. This is accomplished by the DDS 520.

      The Direct Digital Synthesizer (DDS) 520 is used as a fractional divider or fractional phase accumulator that generates a fractional prime sub-multiple of the recovered clock. The DDS 520 translates the wideband recovered clock from any bit rate to a fixed clock feeding the PLL 525. A block diagram of the DDS 520 is shown in

15 Fig. 6 and includes an accumulator 175, a register 620, a memory 630, a Digital to Analog (D/A) converter 640, and a filter 650. The filter 650 can be a low pass filter or a high pass filter.

      The Increment (I) in the DDS block diagram is summed with the previous accumulated value at intervals set by the recovered clock. The upper bits of the output

20 of the register 620 drive the address of a lookup memory table that contains a sine wave signal. The memory 630 output is converted to an analog output using the D/A converter 640, and then filtered from harmonics with the low pass filter 650. The value of the Increment is selected to give an absolute and accurate fixed value for the translated clock. This function makes the under-sampling bit rate agnostic. That is, it

25 can support any bit rate, not just SONET (Synchronous Optical Network), FEC (Forward Error Correction), or 10GE (10 Gigabit Ethernet) rates.

      The DDS 520 functions as a fractional divider. The PLL 525 multiplies the translated clock by a prime fraction, as shown in the following example for 10G rates:

30

Recovered Input Clock	DDS Divider Ratio	Recovered Clock to Sample Clock Ratio
9.95328 GHz	494.16531	62.21125MHz
10.3125Gbps	512.00004	64.453125MHz
10.6642Gbps	529.46141	66.65125MHz
10.709Gbps	531.68567	66.93125MHz

The DDS embodiment generates a sample clock that has a fixed frequency

5 relationship to the time base of the incoming signal. This relationship is illustrated in the timing diagram of Fig. 7.

In relation to a DSP algorithm 710, a counter tracks the order of the samples. The DSP assigns a time domain index for every sample in the memory based on the fractional portion of the following equation:

10

Index = Fraction (SO * SR)

Index = the time domain fraction of the Unit Interval (UI) of a single cycle of input data

SO = the Sample Order from the data registered with the internal counter

SR = the Sample Ratio of frequency of the input signal to the frequency of the Sample

15 Clock

Fraction = the fractional value that results from subtracting round down of (SO*SR) from (SO*SR)

Example:

20 Recovered Input Clock: 9.95328GHz

Sample Clock: 160MHz

Recovered Clock to Sample Clock Ratio: 62.21125

Consecutive samples of the input signal will have the following index and thus

25 corresponding time domain coordinate:

Sample Order	SO * SR	Index or fraction of Unit Interval (UI)
1	62.21125	0.21125
2	124.4225	0.4225
3	186.63375	0.63375
4	248.845	0.845
5	311.05625	0.05625
6	373.2675	0.2675

As a large number of samples is accumulated, distinct values along the x-axis or
time domain axis are collected and used to display and analyze the data.

Fig. 8A shows a block diagram of an embodiment of the sampling circuit 140
shown in Fig. 1. In the amplitude portion 850a of the embodiment, a Track and Hold
(T/H) sampler 830 receives and samples the input signal and an Analog to Digital (A/D)
converter 240 digitizes the output from the T/H Sampler 830. The T/H Sampler 830
and the A/D converter 240 are clocked by a sample clock derived from coherent under-
sampling delayed by a fixed delay 805, e.g., 0.5 to 0.75 UI. Sample values above the
preset high threshold or below the preset low threshold are not considered for extracting
Time Interval information. All other sample values are considered to have occurred
during a transition from Low to High or from High to Low and are used for extracting
Time Interval information.

In the phase portion 850b of the embodiment shown in Fig. 8A, two flip-flops
receive the input signal and produce the digital values Decision Circuit Before (DCB)
and Decision Circuit After (DCA) indicative of phase information. A first flip-flop
810a outputs the DCB value and receives the sample clock derived from coherent
under-sampling delayed by a programmable delay 815 which is adjusted by the delay
control circuit 120 shown in Fig. 1. The programmable delay 815 is adjusted such that
the output value DCB occurs 0.5 unit intervals before the digitized sample output from
the amplitude portion 850a of the embodiment in Fig. 8A. A second flip-flop 810b
outputs the DCA value and receives the same sample clock as the first flip-flop 810a,
but delayed by a fixed one unit interval delay 825. Thus, the output DCA value occurs

0.5 unit intervals after the digitized sample output from the amplitude portion 850a of the embodiment in Fig. 8A. The decision circuit values are then used to determine the phase of the transition according to the following logic: If DCB = 1 & DCA = 0, then High to Low transition; if DCB = 0 & DCA = 1, then Low to High transition.

5   Fig. 8B illustrates possible positions of the sampling instants with respect to the input signal. The phase samples are latched in nominally a half unit interval before and after the amplitude sample as shown in Fig. 8B. The solid horizontal lines represent the preset high and low threshold values within which the amplitude sample must occur to be considered for jitter measurements.

10   Fig. 9 is a block diagram of an athermal embodiment of the sampling circuit 140 shown in Fig. 8A. An Optical to Electrical (O/E) converter 920 in series with a Variable Gain Amplifier (VGA) 925 receive the input signal and provide the electrical signals AIN and DIN to the amplitude and phase portions of the sampling circuit. Unlike the embodiment in Fig. 8A, the first flip-flop 810a and the second flip-flop

15   810b, together forming the flip-flops 810, are thermally coupled with a heat sink 910 to maintain their timing requirements over a wide temperature range. Moreover, the programmable delay 815 coupled to the flip-flops 810 is placed on the line between the sample clock and the T/H sampler 830 and A/D converter 240. The delay control circuit 120 adjusts the delay nominally to 0.5 unit intervals such that the amplitude

20   sample maintains a position 0.5 unit intervals from DCB and DCA. Path length matching of the lines leading from the sample clock to the T/H sampler 830 and the flip-flops 810 applies to maintain the relative phase positions of the amplitude and phase samples.

      Fig. 10 shows a timing diagram illustrating the functions performed by the

25   sampling circuit 140 shown in Fig. 9. AIN is the input signal received by the T/H sampler 830. DIN is the input signal value latched by the flip-flops 810 according to the delayed sample clocks, CA and CB, corresponding to the decision circuit values DCA and DCB, respectively. SC is the Sample Clock and CTH is the sample clock received by the T/H sampler 830. The DIN values obtained at CB and CA correspond

30   to the decision circuit values DCB and DCA, respectively. In the first set of samples

shown in Fig.10, DCB = 1 and DCA = 1, thus there is no transition. In the second set of samples shown in Fig. 4, DCB = 0 and DCA = 1, thus the transition is from Low to High.

Fig. 11 shows another timing diagram of the sampling circuit 140 shown in Fig. 9. The decision circuit data bits, DCA and DCB, are phase samples corresponding to the input signal ideally taken half a unit interval before and half a unit interval after the amplitude sample of the input signal is taken as illustrated in Fig. 11. The middle "x"s shown in Fig. 11 represent the amplitude samples and the adjacent "x"s represent the phase samples. The decision circuit data bits, DCA and DCB, are used to determine whether a Low to High transition or a High to Low transition occurs when the amplitude sample is between preset high and low threshold values. For example, in the fourth set of samples of the NRZ Input the first phase sample is Low and thus DCB = 0 and the second phase sample is High and thus DCA = 1. Therefore, the transition is from Low to High.

Fig. 12 shows a state table 1210 for the state machine implemented in the statistics counter 125 shown in Fig. 1. The statistics counter 125 includes valid, lead, and lag counters. Depending on the state determined from both the amplitude and phase samples, one or more of the counters is incremented and the programmable delays 815 in Fig. 8 and Fig. 9 are adjusted based on the counts in the valid, lead, and lag counters. The scale of the difference in counts between the counters is proportional to the error shift from ideal phase position. Thus, the ideal phase position occurs when the valid, lead, and lag counters have the same value.

The statistics counter also includes an Out Of Lock (OOL) counter and a No Transition (NT) counter. In either the 001 Low or Metastable (L or MS) state or the 110 High or Metastable (H or MS) state, the lag counter is incremented and the delay is decreased. In either the 100 L or MS state or the 011 H or MS state, the lead counter is incremented and the delay is increased. In either the Low to High transition (L-H) or High to Low transition (H-L) states, the valid counter is incremented. In either the High (H) or Low (L) states, the NT counter is incremented. Finally, in the Error states (010 or 101), the OOL counter is incremented.

A state table diagram 1220, also shown in Fig. 12, illustrates each of the states except for the L and H states. The outer triangles represent the phase sample instants and the triangles between the outer triangles represent the amplitude sample instants.

A second athermal embodiment of the sampling circuit 140 (Fig. 1) is shown in

5   Fig. 13. In this embodiment two T/H samplers 830, thermally coupled with a heat sink 910 to ensure common behavior as a function of temperature, receive the input signal. The T/H samplers 830 receive the sample clock separated by a 0.5 unit interval delay 1305. A comparator 1310 compares the output values from the T/H samplers 830 to determine whether an amplitude sample corresponds to a rising or a falling edge.

10   A third athermal embodiment of the sampling circuit 140 (Fig. 1) is shown in Fig. 14. In this embodiment two T/H samplers 830 receive the input signal and two A/D converters 240 receive the outputs from the T/H samplers 830. The T/H samplers 830 and the A/D converters 240 receive the sample clock separated by a 0.5 unit interval delay 1305. The outputs from the A/D converters 240 are fed to a digital signal

15   processor (not shown) which determines whether the amplitude sample corresponds to a rising or falling edge. Either output may be used as an amplitude for jitter measurements.

Fig. 15 shows a logic block diagram of the Time Interval Computation block 160 and Signal Processing block 180 shown in Fig. 1 which extract and perform signal

20   processing on the Time Interval Error (TIE) and the TIE sequence information. The Time Interval Computation block 160 includes logic block diagrams for the transition identification and ideal index calculations. The transition identification is accomplished by comparing the input amplitude sample against preset thresholds (e.g., Hi-(0.2*(Hi-Lo)) and Hi-(0.8*(Hi-Lo))). If the input amplitude sample value is above the low

25   threshold 1505a and below the high threshold 1505b (the "and" logic is shown as a first AND gate 1510a), then the sample is considered to have occurred at a transition (i.e., transition(n) = 1); otherwise, the sample did not occur at a transition (i.e., transition(n) = 0). Ideal_Index(n) is the fraction of the unit interval (a single cycle) of the input signal used as an address to extract data from memory for comparison. Ideal_Index(n) is

30   obtained by summing the fractional portion of M/N, or the ratio of the input signal

frequency to the sampling clock frequency, with Ideal_Index(n-1) using a summer 1530 and extracting the fractional portion from the resulting decimal number using an extract Fraction function block 1525. The transition(n) and ideal_index(n) values connect to the inputs of a second AND gate 1510b so that the ideal_index value does not pass

5   through to the differentiator 1520 unless the amplitude sample occurs on a transition.

        The sampled signal data values provide an address to an NxN look up table for LH_Ideal 410 or an NxN look up table for HL_Ideal 420 containing the ideal rising and falling signal characteristics, where N is the square of the number of bits of the A/D converter 240. A channel selector coupled to a Mux 1515 selects either the H-L or the

10   L-H data to be differentiated. The differentiator 1520 computes the difference between the measured data from the look up table and the Ideal_Index value. In other words, the differentiator computes the difference in time between the measured phase of the signal and where the signal should be if there were no jitter. The output of the differentiator 1520, TIE(n), is the instantaneous value of the jitter in the time domain from the

15   previous sample. This output is accumulated over time by an accumulator 175 to produce a TIE sequence, TIE_Seq(n), which is the time domain representation of the jitter.

        To reduce the memory requirements for wander measurements, an interleaver 1535 skips an integer number of samples (INT) prior to storing the data in memory

20   1540. Next, the digital signal processor (DSP) 185 computes the spectral domain characteristics of the TIE sequence by means of the Fast Fourier Transform (FFT) or the Discrete Fourier Transform (DFT). Moreover, to obtain the peak to peak jitter, a peak detector 1545 captures the positive and negative maximum values of the TIE sequence.

        Fig. 16 shows an algorithm or Boolean logic corresponding to the logic blocks

25   in Fig. 15 which extract the TIE and the TIE sequence.